

MONOLITHIC GPS RF FRONT END INTEGRATED CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application claims priority under 35 U. S. C. § 119(e) of United States Provisional Patent Application No. 60/221,048, filed July 27, 2000, entitled "MONOLITHIC GPS RF FRONT END IC WITH FULLY INTEGRATED VCO AND IF FILTER" by Robert Tso et al., which application is incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

10 The present invention relates in general to Global Positioning System (GPS) receivers, and in particular to a GPS Radio Frequency (RF) front end Integrated Circuit (IC) with a high level of monolithic integration.

2. Description of the Related Art.

15 GPS receivers, once used primarily for military and surveying applications, are finding new uses in the commercial arena. Location services, emergency location using 911 (E911) phone calls for cellular telephones, personal GPS receivers, etc. are all part of current and emerging products and services enabled by using GPS receivers.

20 A typical GPS receiver uses an RF-IF/Converter section that selects, amplifies, filters, downconverts the received GPS signals, and a baseband processing section to despread and detect the downconverted signals and determine a position of the GPS receiver. The RF section of

today's GPS receivers are designed by each company that makes the receiver, and therefore, there are no established standards for such designs.

The analog RF designs typically comprise a Low Noise Amplifier (LNA) section with a two pole bandpass or preselect filter on the input, output, or both, followed by a single, double, or triple conversion receiver topology. The output of the last Intermediate Frequency (IF) section can be an amplitude limited Phase Modulated (PM) signal, which is typically called a 1 bit signal, or it can be a 2 bit system, typically consisting of a magnitude signal and sign signal. The analog RF section can also be partitioned at the output of a ≥ 2 bit A/D converter. The last IF stage may contain a limiter for a 1-bit system, or Automatic Gain Control (AGC) may be used to allow limiting to be performed by the ≥ 2 bit A/D converter.

For a single conversion receiver, the IF filtering usually follows an image reject mixer, and is typically a ≥ 2 pole design. The IF filter can be a balanced design to achieve common mode noise rejection, or be a single ended filter. The typical image rejection performance of the image reject type mixer is approximately 20 dB or better, which is adequate for GPS.

A double conversion receiver typically comprises an LNA, an image rejection filter, a mixer, a first IF image rejection filter, a second mixer, and the final IF filter, and amplifier.

The gain of these systems is usually selected to be as small as feasible, while still allowing the final IF amplifier to achieve the desired output level, allowing for component variation. The gain of this system is typically governed by the noise bandwidth of the entire receive chain, that is the gain of the system is as needed to take in the noise power at the input, filter it, and then drive the receiver output to the proper levels.

The oscillator and/or frequency synthesizer sections of these receivers generate the desired timing, sampling, and mixer LO frequencies needed to downconvert the input RF signal to the

proper IF frequencies. The necessary frequencies generated vary from design to design, and are generally unique to each receiver. Historically there has been little consistency among designs of GPS receivers. One common trait is that the input reference frequency must be very stable in terms of short term noise, or else the GPS signal processing will experience deleterious cycle slips in the signal tracking loops, resulting in loss of lock or other forms of impaired receiver performance.

A highly integrated RFIC that is compatible with the frequency plan disclosed in United States Patent No. 5,897,605, which is incorporated by reference herein, provides utility in the implementation of GPS receivers.

Because there is little consistency between GPS receiver designs, it is difficult to design an RF portion of the GPS receiver that is compatible with more than one baseband processing section of a GPS receiver. Further, difference in frequency plans for GPS receivers make the RF portion and the baseband processing sections of different GPS receivers incompatible.

It can be seen, then, that there is a need in the art for a GPS receiver that can accept the RF GPS signal and convert it to a form that can be applied to a digital processing section, typically implemented as a GPS Processor ASIC. It can also be seen that there is a need in the art for a GPS RF front end that can be implemented primarily in a monolithic RFIC requiring a minimum of external components. It can also be seen that there is a need in the art for a GPS RF front end that uses receiver topologies that can be implemented using standard building blocks.

SUMMARY OF THE INVENTION

To minimize the limitations in the prior art, and to minimize other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a receiver topology that is easily integrated from industry standard building blocks. With the broad variation in potential receiver designs, the present invention includes some specific receiver topologies that lend themselves to a high level of integration. The specific designs presented here are comprised of industry standard building blocks and functions that have been described elsewhere in the related art.

An apparatus in accordance with the present invention comprises the RF/IF-Converter portion of a GPS receiver. The RF/IF-Converter portion is embodied in an RFIC that includes an image rejection combining filter, wherein the noise bandwidth of the GPS receiver is set by the IF active filter, an Automatic Gain Control (AGC) amplifier, an Analog-to-Digital Converter (ADC), and a frequency synthesizer section.

It is an object of the present invention to accept the RF GPS signal and convert it to a form that can be applied to a digital processing section, typically implemented as a GPS Processor ASIC.

It is another object of the present invention to provide a GPS RF front end that can be implemented primarily in a monolithic RFIC requiring a minimum of external components. It is another object of the present invention to provide a GPS RF front end that uses receiver topologies that can be implemented using standard building blocks.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIG. 1 illustrates a typical GPS position determination system;

FIG. 2 illustrates a GPS RF front end in accordance with the present invention;

FIG. 3 is a block diagram illustrating an alternative embodiment of the GPS RF front end of the present invention; and

FIG. 4 is an illustration of the interface between the RF front end and the digital processing section of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

In the following description of the preferred embodiment, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other
5 embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

GPS Overview

FIG. 1 illustrates the essential elements of a GPS position determination system.

10 System 100 comprises several GPS satellites 102A-102C. Each GPS satellite 102A-102C emits signals 104A-104C respectively, which are spread-spectrum Radio Frequency (RF) signals in the L-band of the RF spectrum. These signals contain information regarding satellite 102A-102C identification (also known as SV number), time of transmission of the signal, etc. More
15 information regarding the data content and structure of the signals can be found in "The Navstar Global Positioning System" by T. Logsdon, which reference is incorporated by reference herein. Three GPS satellites 102A-102C and three signals 104A-104C are shown for illustrative purposes only; system 100 comprises typically twenty-four operational satellites at different orbits, such that several satellites are typically visible to any given point on the earth at any specific time.

At least one of the signals 104A-104C is received at a GPS receiver 106, which typically
20 comprises an RF Front End 108 and a digital Application Specific Integrated Circuit (ASIC) 110. The GPS RF Front End 108, downconverts the L-band signals 104A-104C to a lower frequency and the digital ASIC 110 performs correlation, detection and demodulation of the GPS signals 104A-104C to determine a distance between the GPS receiver 106 and each of the satellites 102A-

102C, depending on which signals 104A-104C are received. For example, if only signals 104A and 104B are received by GPS receiver 106, then the distance between GPS receiver and GPS satellite 102C is not computed by GPS receiver 106. These distances are determined by comparing a clock located in the GPS receiver with the demodulated time data determined from the signals 104A-104C that have been received by the GPS receiver 106, and from the equation distance = rate x time, distance is determined, because the signals 104A-104C travel at a rate equal to that of the speed of light. These distances are known as “pseudoranges” because certain errors have not been removed from the distance calculations.

More complex GPS receivers 106 take into account certain errors in the distance determinations derived from signals 104A-104C. For example, the clock in the GPS receiver 106, typically called the “realtime clock”, but can also be part of the RF front end 108, may have certain errors associated with it, the GPS satellites 102A-102C may not be in their exact orbital slot, there may be ionospheric conditions that affect the distance calculation, and other factors. Given the positions of each satellite and having determined distances to satellites have been determined by the GPS receiver 106, the GPS receiver 106 can then output a longitude and latitude position of the GPS receiver 106. Typically, two to four distances must be calculated by the GPS receiver 106 to determine the position of GPS receiver 106.

The GPS Receiver

FIG. 2 illustrates a GPS RF front end in accordance with the present invention.

Figure 2 illustrates RF front end IC 107, which includes monolithic and discrete elements. The electronics of the GPS receiver 106 are typically implemented as a fully custom Radio Frequency Integrated Circuit. (RFIC), coupled to a GPS processor or GPS engine implemented

using digital ASIC technology. One such GPS engine is described in U.S. Patent No. 5,897,605, which is incorporated by reference herein. The GPS signals 104A-104C are typically received by a GPS antenna 200, and are then applied to an LNA or section 202. The LNA 202 may be fully included in the RFIC or may be distributed between the RFIC and an external amplifier, to achieve a better noise figure. The LNA section may have an input filter to limit unwanted signals which may cause receiver interference. The LNA may use an output filter 204 to limit the unwanted out of band signals. U.S. Patent No. 4,701,934, issued to Jasper, which is incorporated by reference herein, presents a system where the LNA output filter 204 is used as the receiver noise bandwidth setting filter, but in the implementation described in the Jasper patent, this filter 204 is also used to attenuate out of band intermodulation products and high level out of band spurious signals that could cause receiver 106 performance degradation.

In the present invention the noise bandwidth of the receiver 106 is set in the IF filter 206 following the image reject mixer 208. In the preferred embodiment, the 6 dB bandwidth of the IF filter 206 is nominally 6 MHz. The output from the internal LNA 210 is applied to the input of an image reject mixer 208. The image reject mixer 208 comprises 2 double-balanced mixers 212 and 214 with In-phase LO (I-LO) and Quadrature-phase LO (Q-LO) inputs, and I-IF and Q-IF outputs, I and Q Active Filter Circuits 206 and a combiner circuit (phase shift network) 216. The I-IF and Q-IF outputs are combined using phase shift network 216 to obtain a single IF output. The L1 GPS signal, which is centered at 1575.42 MHz is down-converted to the IF frequency at approximately 9.5 MHz by an image reject mixer. The IF AGC amplifier boosts the IF signal to the proper level for quantizing by a 2 bit A/D converter. The IF AGC amplifier 218 gain is controlled from the digital processing section in the digital ASIC, by way of AGC control block 220. The sample clock for the A/D converter 222 is provided by the ACQCLK signal, which is

generated by the Divide by 41 section 224 which is synthesized by a Phase Locked Loop (PLL) locked to the crystal oscillator 226, which provides a reference signal. Typically, the ACQCLK signal has a frequency approximately equal to $37.3333f_0$, where $f_0 = 1.023$ MHz. In the preferred embodiment, the digitized GPS information bearing signal is provided as 2-bit Positive ECL (PECL) levels by PECL buffers 254, 256 and sent to the digital ASIC 110.

The synthesizer section 227 of the RF front end 107 is typically entirely contained in the RFIC except for the loop filter components 228, and the support components of the crystal oscillator active circuitry 230. The crystal oscillator section can be implemented using a crystal resonator 226, or using a signal from an external Temperature Compensated crystal Oscillator (TCXO). The crystal resonator 226 frequency is typically nominally 24.5535 MHz, and can vary by 40 parts per million (ppm) around this frequency. The reference oscillator 230 frequency is doubled by frequency doubler 232 and then divided by 9 by divider 234. Of course, the crystal oscillator 230 can generate a frequency of twice that of 24.5535 MHz, which eliminates the need for the frequency doubler 232. The doubled frequency (or direct frequency if it is already generated) is also sent to a PECL output buffer to provide a signal 236, typically named GPSCLK, which is a GPS clock signal used by the digital ASIC 110. Typically, GPSCLK has a frequency approximately $48f_0$, where $f_0 = 1.023$ MHz. The divided-by-9 signal is applied to a phase/frequency detector 238 as the reference input of the phase-lock-loop.

A voltage controlled oscillator (VCO) 242 that operates at a typical nominal frequency of 1565.97 MHz is implemented entirely within the RFIC, and provides 3 output signals. A monolithic VCO, such as described in U.S. Patent No. 5,917,383, which is incorporated by reference herein, may be used. The I and Q outputs of this oscillator 242 are sent to the mixers 212 and 214, and the P output 244 to a divider 224. This divider takes the output signal of the VCO

244 and divides it by 41. The output of this divider is used as the 2-bit A/D sample clock, and is also provided as an RFIC output, ACQCLK. The divider 224 output is also further divided by 7 at divider 246 with output of 246 sent to the phase frequency detector as the feedback signal for the phase-locked loop (PLL) synthesizer.

5 The output of the phase/frequency detector is applied to a charge pump section 240. The charge pump is internal to the RFIC, with the loop filter 228 implemented externally to the RFIC, with passive components. The output of the loop filter is used to control the frequency and phase of signals provided by VCO 242.

10 The sampled SIGN and MAG digital signals 248 and 250, respectively, are provided to PECL buffers to send the signal to the GPS digital ASIC 110 for digital processing. The near one-quarter ratio of the IF signal frequency and the ACQCLK signal frequency 252 allow for easy generation of “near baseband” I and Q signals representing the GPS signal using the sampling and decimation method described in the aforementioned 5,897,605 patent. Interface buffers 254-260 are used to provide PECL signals to the GPS digital ASIC 110.

15 The system of the present invention is differentiated from the system described in the Jasper patent in the generation and control of the LO, the IF filtering, the image reject mixing, the A/D conversion process, and that the RFIC of the present invention is designed to be implemented with very a high level of integration. This is accomplished by setting the noise bandwidth of the receiver 106 using the IF filter 206 following the dual mixers 208.

20 FIG. 3 illustrates a second implementation of the invention.

In FIG. 3, bias control 300 is used to power down portions of RFIC 108 depending on which circuits within the RFIC 108 are needed to receive and/or process signals as determined from the digital ASIC 110, or some other portion of receiver 106. For example, since the

implementation of RF front end 108 shown in FIGS. 2 and 3 use an IF filter section, which comprises mixer 208, Filter 206, and combiner 216 typically use an IF frequency centered at about 9.5 MHz, such an approach allows some of these sections, namely everything shown in FIG. 3 except the crystal oscillator 230, the X2 frequency doubler 232, and the GPSCLK PECL drivers 260 and reference 262 to be turned off when not needed, e.g., when the GPS signals 104A-104C are not being received, but a processing clock is still required for processing the signals on the digital ASIC 110. This approach minimizes the power consumption of the portion of receiver 106 shown in FIG. 3, depending on the state of the RF front end 107.

Interface

FIG. 4 is an illustration of the interface between the RF front end and the digital processing section of the present invention.

As described herein, the present invention allows for a PECL interface between the RF front end 108 IC and the digital ASIC (processing section) 110 for some signals. Such an interface comprises an acquisition clock (ACQ CLK or CLK ACQ) signal 400, a GPS Clock (GPS CLK or CLK GPS) signal 402, a SIGN signal 404, a MAG signal 406, and a reference (PECL REF or REF) signal 408. The interface also comprises non-PECL signals from the digital ASIC 110 to the RFIC 108, such as a AGC Data (AGC DATA or AGCDAT) signal 410. The interface may also comprise a power management (PWR MGMT) signal 412 that is usually input into the bias control 300. Signal 412 is typically used to turn the RF front end 108 on and off based on the needs of the receiver or system. The power management signal 412 is typically a low bandwidth, low-power signal, such as a CMOS control signal.

The interface of the present invention couples the RF front end 107 to the digital processing section 110, which processes the signals 400-410 and determines a position of the GPS receiver 106. Since the interface uses PECL compatible signals for the clock and data signals there will typically be less interference generated by signals in the interface, than if the interface employed TTL or CMOS compatible signals.

Conclusion

Although the description of the present invention herein describes specific embodiments of the present invention, the scope of the present invention includes other embodiments of the present invention not described herein. For example, there are other combinations of a GPS receiver possible given the LNA, mixer, amplifier, VCO, and other functions described in the systems presented in FIGS. 1 and 2 that do not substantially change the systems described above. Those skilled in the art will also realize that minor variations of the reference frequencies and filter bandwidths are within the scope of the present invention. Those skilled in the art will also realize that implementing the RF front end described above in different semiconductor technologies, e.g., different materials such as Gallium Arsenide, bipolar, CMOS, NMOS, PMOS, BiCMOS, or other circuit methodologies, is still within the scope of the present invention.

In summary, the present invention describes an apparatus that functions as the RF portion of a GPS receiver. The RF front end comprises an RFIC that includes a single stage downconverter using dual mixers, an I/Q Intermediate Frequency (IF) active filter, an I/Q Combiner, an Automatic Gain Control (AGC) IF amplifier, an Analog-to-Digital Converter (ADC), and a frequency synthesizer section, wherein the noise bandwidth of the GPS receiver is set by the IF active filter.

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